AMENDMENT TO THE SPECIFICATION:

Please amend the paragraph on page 4, lines 11-30, as follows:

FIG. 1 depicts a block diagram of a receiver device 100 consistent with certain embodiments. In this exemplary embodiment, a DSSS signal is received at antenna 104 and passed to a frequency converter circuit 108 for down-conversion. The frequency converter (e.g., mixer) 108 utilizes a local oscillator in the form of a non-crystal based frequency generator 112 which produces a signal which is mixed with the incoming signal from antenna 104 to produce the output of the frequency converter 108. This output from the frequency converter is coupled to a differential chip detector 116, which is defined herein as a detector circuit. ~~that operates according to the principles described in U.S. Patent No. 6,563,857, filed December 21, 2001, entitled "Low Cost DSSS Communication System."~~ Differential chip detection as described in this patent application is ~~also~~ described in detail in Q. Shi, R. J. O'Dea, and F. Martin, "A New Chip-Level Detection System for DS-CDMA," 2002 IEEE International Conference on Communications, vol. 1, pp. 544-547, 2002. ~~These documents show~~ This document shows that differential chip detection can increase the tolerance of a receiver to frequency offset. However, it was not recognized that the same mechanism could also be utilized to mitigate the effect of low-frequency noise (i.e., phase noise / close-in noise) on the receive Local Oscillator (LO) or transmit carrier signal, thus facilitating use of a crystal-less oscillator. The mitigation of low frequency noise on the local oscillator and/or carrier oscillators will be explained and proven in the discussion accompanying **FIG. 5**.